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- ,2016.



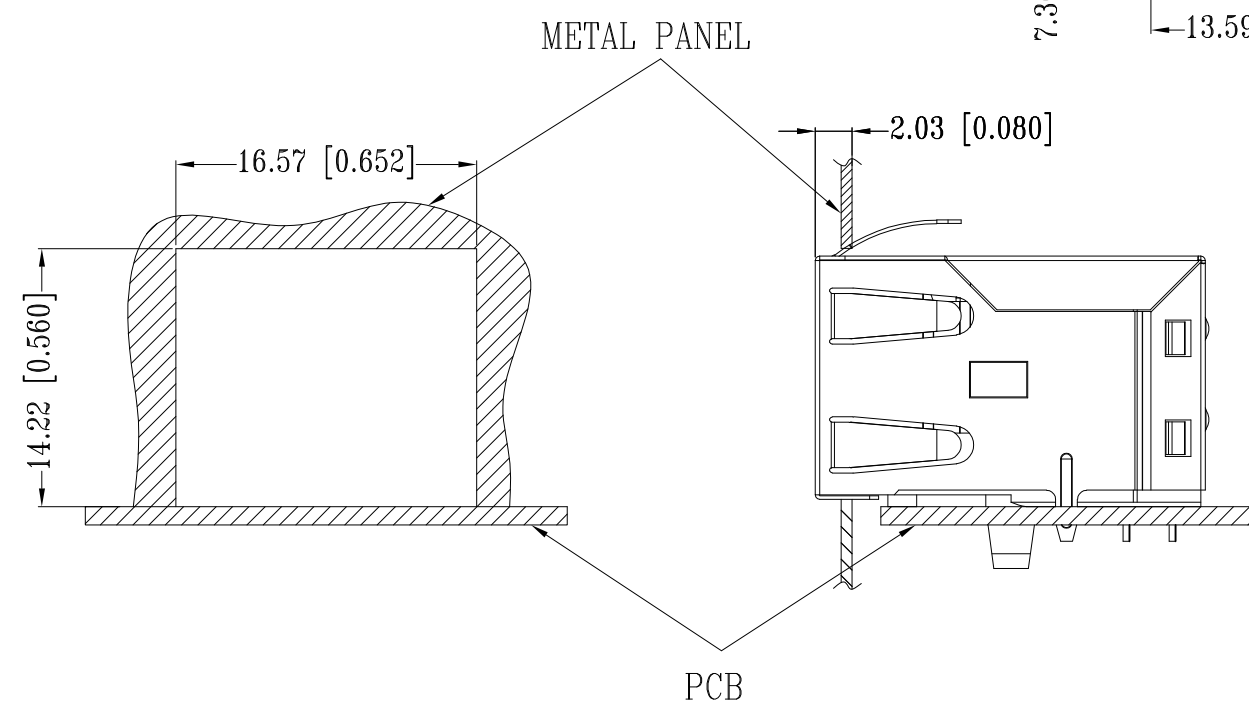
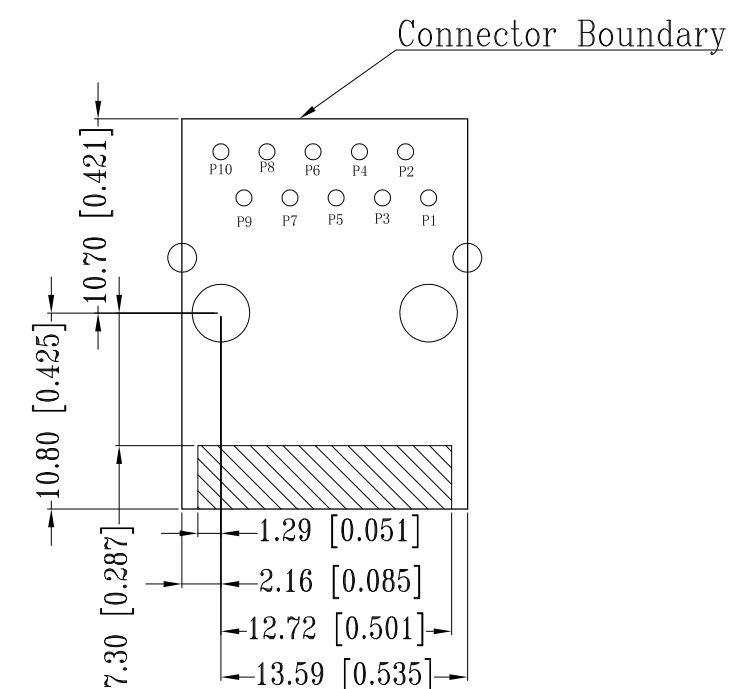
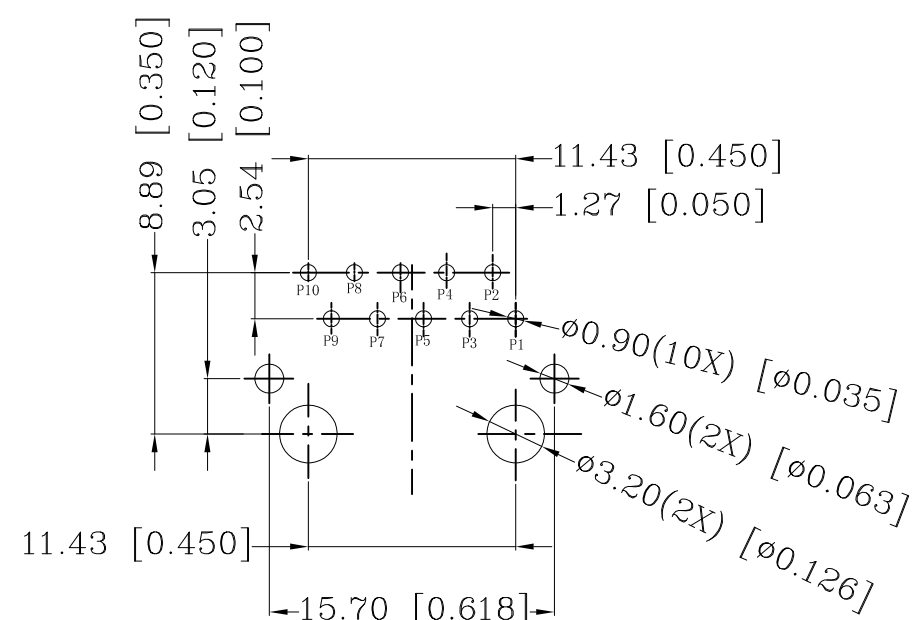
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REVISIONS

P	LTR	DESCRIPTION	DATE	DWN	APVD
	-	SEE SHEET 1	-	-	-

SUGGESTED PCB LAYOUT



UNIT: mm / inch
TOLERANCES: ± 0.10 / 0.004

THIS DRAWING IS A CONTROLLED DOCUMENT.

DIMENSIONS:
mm [INCHES]TOLERANCES UNLESS
OTHERWISE SPECIFIED:

0 PLC $\pm -$
1 PLC $\pm -$
2 PLC $\pm -$
3 PLC $\pm -$
4 PLC $\pm -$
ANGLES $\pm -$



MATERIAL



FINISH



DWN 02AUG2016

GANESH C M

CHK 02AUG2016

FRANZ MUELLER

APVD 02AUG2016

MARTIN SZELAG

PRODUCT SPEC

108-94552

APPLICATION SPEC

114-94447

WEIGHT

0

CUSTOMER DRAWING



TE Connectivity

NAME

RJ45 JACK INT.MAG. 1Gb 1x1

SIZE

A3

CAGE CODE

00779

DRAWING NO

C-2301994-5

RESTRICTED TO

-

SCALE 3:1

SHEET 2 OF 3

REV B1

4

3

2

1

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REVISIONS

P	LTR	DESCRIPTION	DATE	DWN	APVD
	—	SEE SHEET 1	—	—	—

ELECTRICAL CIRCUIT DIAGRAM

P1

CAP 1000pF/2kV

75 Ω

75 Ω

75 Ω

75 Ω

P2

P3

P5

P6

P4

P7

P8

P9

P10

1CT:1CT

1CT:1CT

1CT:1CT

1CT:1CT

1CT:1CT

1CT:1CT

1CT:1CT

1CT:1CT

J8

J7

J5

J4

J6

J3

J2

J1

1.0 Turn Ratio @100kHz: (P9~P8):(J1~J2) = 1:1±2%
(P7~P4):(J3~J6) = 1:1±2%
(P6~P5):(J4~J5) = 1:1±2%
(P3~P2):(J7~J8) = 1:1±2%

2.0 Primary Inductance: 350μH MIN. @100kHz, 0.1V 8mA DC BIAS

3.0 DC Resistance: 1.2 OHMS MAX.

4.0 Insertion Loss: 1–100MHz –1.0dB MAX.
100–125MHz –1.2dB MAX.

5.0 Return Loss: 1–40MHz –16dB MIN.
40–60MHz –12dB MIN.
60–80MHz –10dB MIN.
80–100MHz –8dB MIN.

6.0 CROSS TALK: 1–100MHz –30dB MIN.

7.0 COMMON TO COMMON MODE ATTENUATION: 1–100MHz –30dB MIN.

8.0 Isolation: PHY Side to Line Side: 2250VDC

2301994-5

WWYY-xxxx

TE

FCC

CONTROL CODE

DATE CODE

"0213"

YY-YEAR

WW-WEEK

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DIMENSIONS:
mm [INCHES]

0 PLC ± –
1 PLC ± –
2 PLC ± –
3 PLC ± –
4 PLC ± –
ANGLES ± –

FINISH

7

1

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SHEET 3 OF 3

REV B1

1470-19 (1/15)