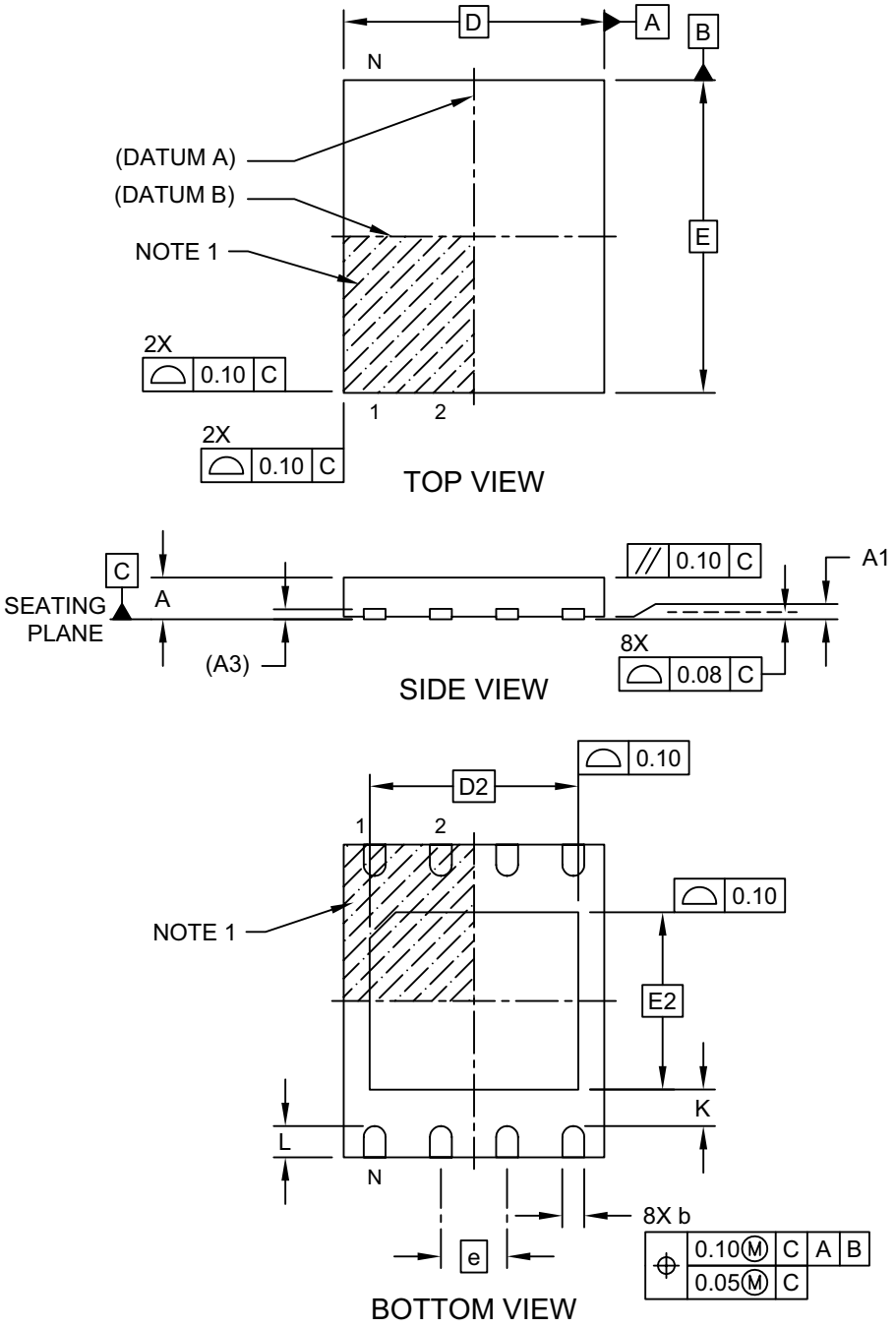
8-Lead Very, Very Thin Small Outline , No Lead Package (EZX) - 5x6 mm Body [WSON]

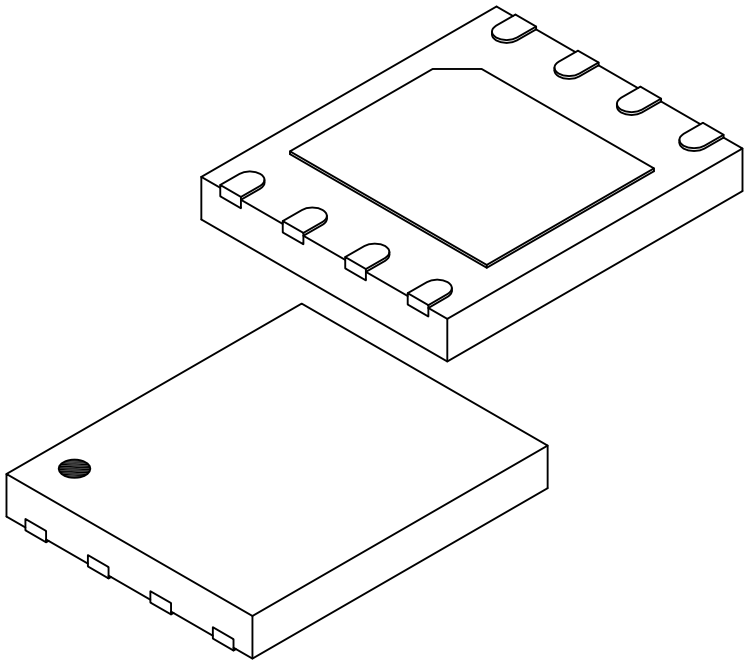
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-452A Sheet 1 of 2

8-Lead Very, Very Thin Small Outline , No Lead Package (EZX) - 5x6 mm Body [WSON]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2		4.00 BSC	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2		3.40 BSC	
Terminal Width	b	0.35	-	0.48
Terminal Length	L	0.50	0.60	0.70
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

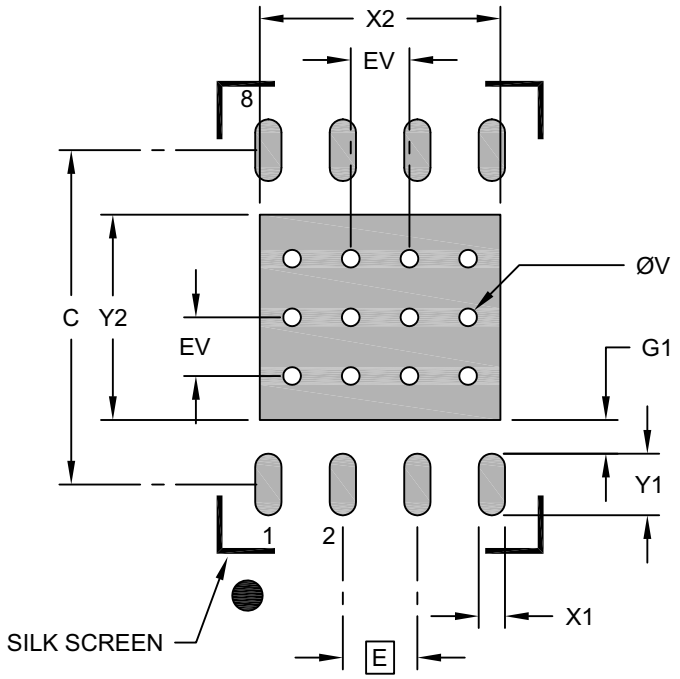
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

8-Lead Very, Very Thin Small Outline , No Lead Package (EZX) - 5x6 mm Body [WSON]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Optional Center Pad Width	X2			4.10
Optional Center Pad Length	Y2			3.50
Contact Pad Spacing	C		5.70	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.05
Contact Pad to Center Pad (X8)	G1	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2452A