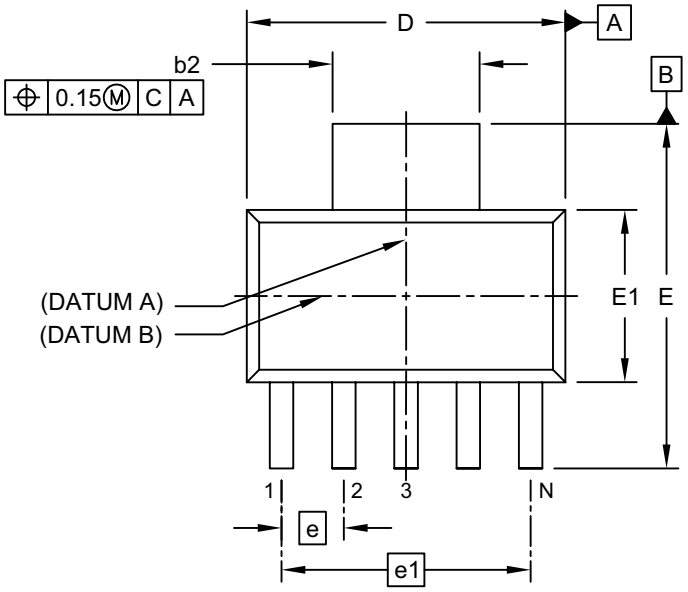
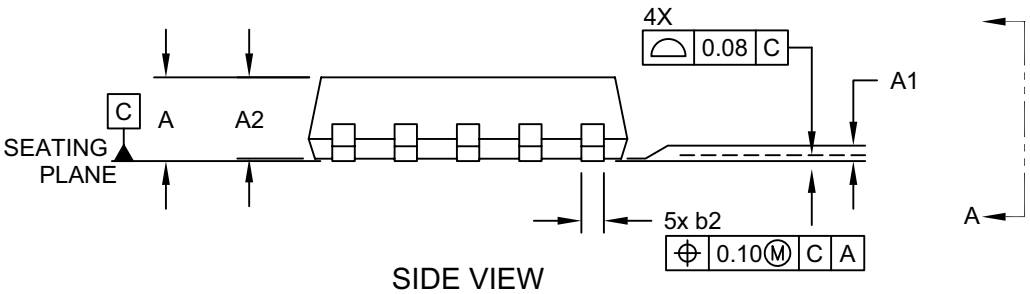
5-Lead Plastic Small Outline Transistor (DC) [SOT-223]

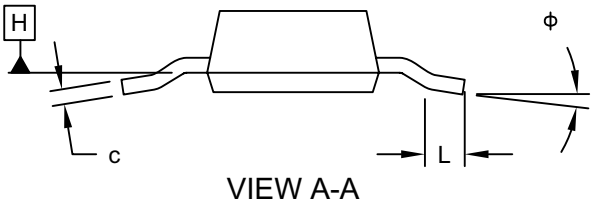
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



VIEW A-A

5-Lead Plastic Small Outline Transistor (DC) [SOT-223]

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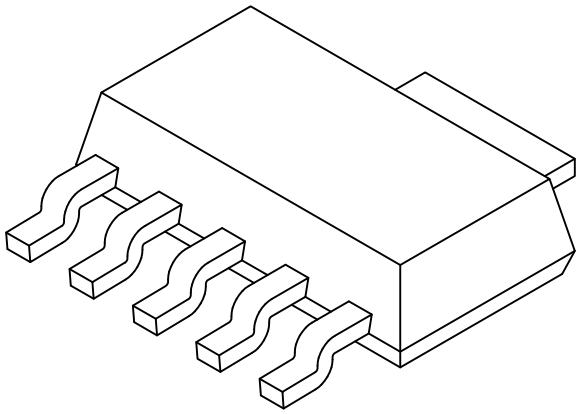

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		5	
Lead Pitch	e		1.27 BSC	
Outside lead pitch	e1		5.08 BSC	
Overall Height	A	-	-	1.80
Standoff	A1	0.02	0.06	0.10
Molded Package Height	A2	1.55	1.60	1.65
Overall Width	E	6.86	7.00	7.26
Molded Package Width	E1	3.45	3.50	3.55
Overall Length	D	6.45	6.50	6.55
Lead Thickness	c	0.24	0.28	0.32
Lead Width	b	0.41	0.46	0.51
Tab Lead Width	b2	2.95	3.00	3.05
Foot Length	L	0.91	-	-
Lead Angle	ϕ	0°	-	10°

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

5-Lead Plastic Small Outline Transistor (DC) [SOT-223]

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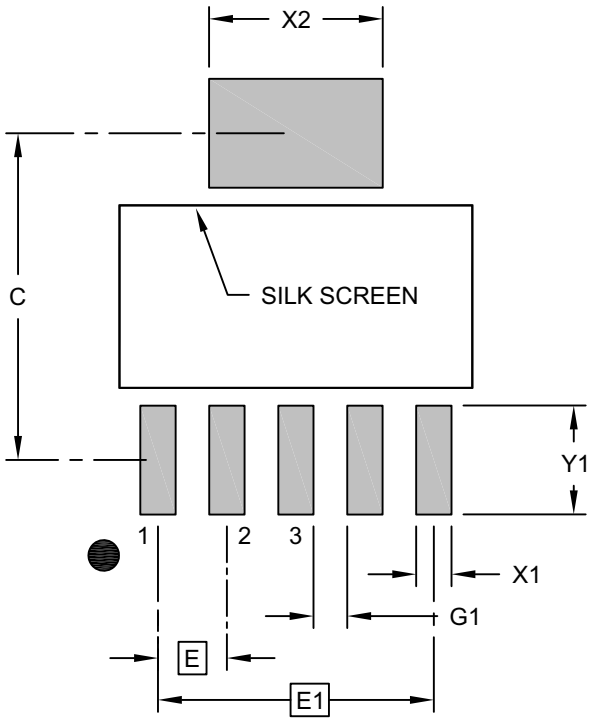

RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pitch	E1	5.08 BSC		
Contact Pad Spacing	C		6.00	
Contact Pad Width (X5)	X1			0.65
Contact Pad Width	X2			3.20
Contact Pad Length (X6)	Y1			2.00
Distance Between Pads (X4)	G1	0.62		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2137 Rev B