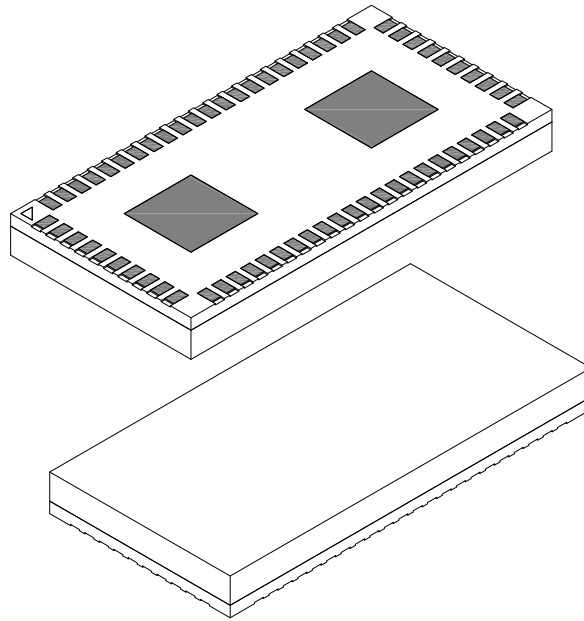


64-Lead Very Thin Fine Pitch Land Grid Array (JVC) - 10x5x1.0 mm Body [VFLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



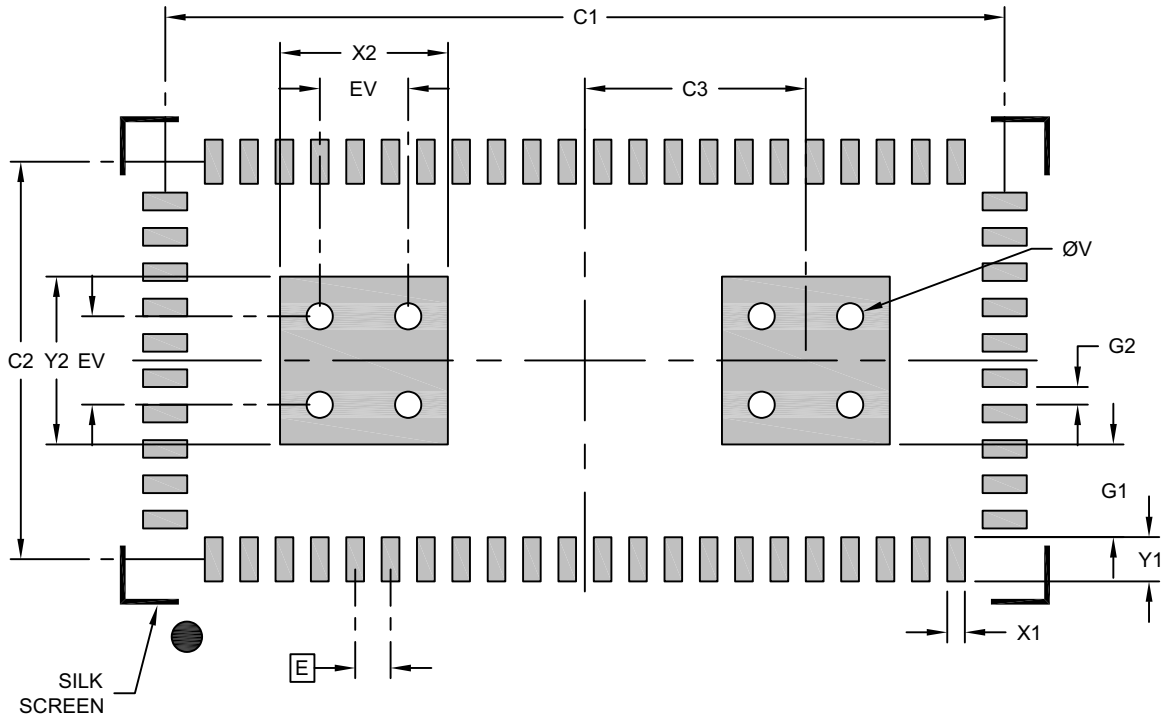
Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	64		
Pitch	e	0.40 BSC		
Package Center to Terminal Center (X2)	eD	4.70 BSC		
Package Center to Terminal Center (X2)	eE	2.20 BSC		
Overall Height	A	–	–	1.00
Substrate Thickness	A1	0.19 REF		
Mold Cap Thickness	A2	0.70 REF		
Overall Length	D	10.00 BSC		
Exposed Pad Length (X2)	D2	1.80	1.85	1.90
Package Center to Exposed Pad Center (X2)	K	2.50 BSC		
Overall Width	E	5.00 BSC		
Exposed Pad Width (X2)	E2	1.80	1.85	1.90
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal Pullback	L1	0.10 REF		

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.

64-Lead Very Thin Fine Pitch Land Grid Array (JVC) - 10x5x1.0 mm Body [VFLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.40 BSC		
Center Pad Width	X2			1.90
Center Pad Length	Y2			1.90
Contact Pad Spacing	C1		9.50	
Contact Pad Spacing	C2		4.50	
Package Center to Pad Center (X2)	C3		2.50	
Contact Pad Width (X64)	X1			0.20
Contact Pad Length (X64)	Y1			0.50
Contact Pad to Center Pad (X64)	G1	1.05		
Contact Pad to Contact Pad (X60)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process