VSC8501 and VSC8502
Application Note
ENT-AN1232 Advanced Quad Flat No-Lead (aQFN) Package
Surface Mount Assembly Guidelines

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1 Revision History 1.0

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was the first publication of this document.

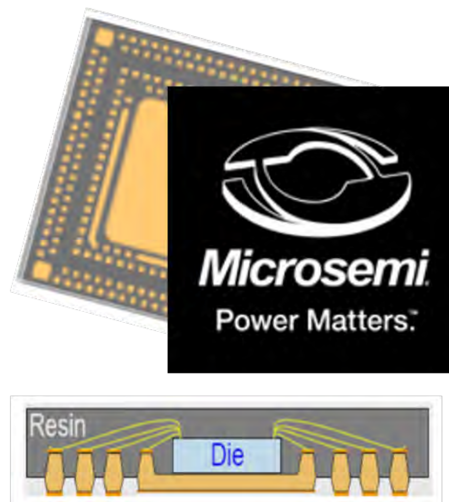
2 Overview

The purpose of this document is to provide surface mount guidelines for the 12 mm × 12 mm, 135-lead Advanced Quad Flat No-Lead (aQFN) package used for the Microsemi Ethernet PHYs VSC8501 and VSC8502.

The aQFN package is a near CSP plastic encapsulated package with a copper leadframe substrate. This package is an extension to the single Row Quad Flat Pack (QFN) leadless package where electrical contact to the printed circuit board (PCB) is made by soldering the lands on the bottom surface of the package to the PCB. The aQFN package has multi-row lands allowing for higher I/O count. The higher standoff has better board-level reliability. The exposed die attached paddle on the bottom is directly attached to the PCB, efficiently conducting heat and providing a stable ground through down bonds and electrical connections through conductive die attach material.

The following illustration shows a cross section for the aQFN package.

Figure 1 • aQFN Package and Cross Section



For optimum thermal, electrical, and board-level performance, special design considerations are required for the PCB and package. The exposed pad on the package needs to be soldered to the PCB using a corresponding thermal pad on the PCB. Furthermore, for proper heat conduction through the board, thermal vias need to be incorporated in the thermal pad design. The PCB footprint design needs to be considered from dimensional tolerance due to package, PCB, and assembly.

3 PCB Design

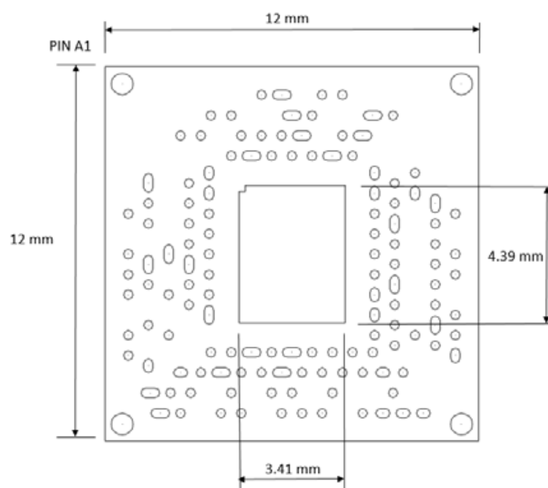
The aQFN package has lands as the terminals. The electrical connection between the package and the PCB is made by printing solder paste on the PCB and reflowing it after component placement.

The following section includes detailed PCB land pattern information and center exposed pad layout guidelines. Stencil information and rework procedures are mentioned in Surface Mount Guidelines (see page 5).

3.1 Package Land Pattern

The following illustration shows the top view of the package land pattern.

Figure 2 • Component Land Pattern (top view)



The package body size is 12 mm × 12 mm. The exposed paddle is 4.39 mm × 3.41 mm and tied to VSS.

There are 4 large circular lands at each package corner. These circular lands are 0.7 mm in diameter. These lands are “no-connect” lands and are needed to provide better board level reliability.

The signal lands are up to 5 rows deep. These pads are placed at 0.65 mm pitch (center-to-center of pads). The lands are depopulated and have the three following sizes:

- Small circular lands at 0.3 mm diameter
- Oval lands at 0.3 mm × 0.45 mm
- Oval lands at 0.3 mm × 0.6 mm

The small circular lands are for signals. The oval lands are for allowing internal multiple wire bonding for power or ground supplies. The depopulation of the lands allows routing on the PCB using low-cost 4 mils PCB line and 5 mils PCB space rules.

Microsemi application engineers can provide a CAD file of the package outline drawing that shows the exact coordinates of the package lands. It is recommended to use the CAD file to get the accurate placement of the package lands.

3.2 PCB Land Pattern

The printed circuit board (PCB) pad pattern follows the same pattern as the package. There are two basic types of PCB land pads: non-solder mask defined (NSMD) and solder mask defined (SMD). NSMD landing pads are recommended because of tighter dimensional controls of the copper etching process than the solder masking process. NSMD landing pads also improve solder joint reliability because solder wraps around the side of the metal pads. The clearance of the solder mask opening and the PCB lands is 50 um.

The metal of the PCB lands follows the same shape as the package, but the lands are made larger. The circular lands on the PCB are 25 um larger than the circular land on the package. The oval lands on the PCB are the same size as the oval lands on the package.

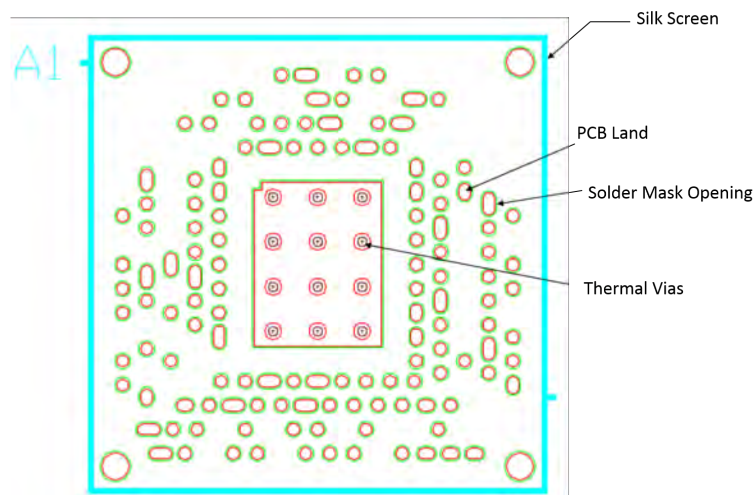
3.3 Center Exposed Pad

The center exposed pad on the PCB is 4.39 mm × 3.41 mm. This is the same size as the exposed pad on the package. The exposed pad on the PCB is NSMD. The solder mask opening is 4.49 mm × 4.51 mm with solder mask-to-metal clearance as 50 um. There should not be any solder mask on the exposed pad of the PCB (this is to maximize thermal dissipation).

Thermal vias are needed to conduct the heat from the paddle through the inner layers of the PCB. The thermal vias are 0.254 mm in diameter and arranged in a 4 × 3 matrix at 1.2 mm pitch. The recommended via plating is 1 oz copper. More thermal vias can be added if design rules allow. If tenting of the vias are required, it's recommended that this be on the top side of the PCB.

The following illustration shows the PCB land pattern.

Figure 3 • PCB Land Pattern



4 Surface Mount Guidelines

A reliable surface mount for the aQFN package depends on an optimal stencil design and paste printing. Care must be taken to form reliable solder joints on the lands, as well as to minimize voids on the exposed paddle.

4.1 Stencil Design

The stencil apertures for the lands have a 1:1 ratio for the oval lands. The stencil apertures for the circular land opening are slightly larger to have better solder joint shape and better joint reliability. The four "no-connect" stencil openings are 0.74 mm, and the small signal stencil opening is 0.34 mm.

The following table lists the dimensions for the package land, PCB land, solder mask opening, and stencil aperture opening.

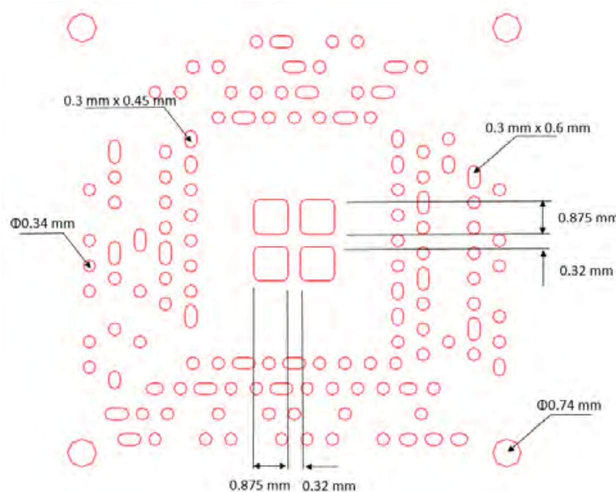
Table 1 • Land Dimensions

	"NC" Pads	Signal Pads	VSS/PWR Pads	VSS/PWR Pads	Exposed Paddle
Package land	ϕ0.7 mm	ϕ0.3 mm	0.3 mm × 0.45 mm	0.3 mm × 0.6 mm	4.39 mm × 3.41 mm
PCB land	ϕ0.725 mm	ϕ0.325 mm	0.3 mm × 0.45 mm	0.3 mm × 0.6 mm	4.39 mm × 3.41 mm
Solder mask opening	ϕ0.825 mm	ϕ0.425 mm	0.4 mm × 0.55 mm	0.4 mm × 0.7 mm	4.49 mm × 3.51 mm
Stencil aperture	ϕ0.74 mm	ϕ0.34 mm	0.3 mm × 0.45 mm	0.3 mm × 0.6 mm	0.875 mm × 0.875 mm

The center paddle stencil aperture has 4 small square openings of 0.875 mm × 0.875 mm. The 4 openings are spaced with a web of 0.32 mm. The corners of the stencil aperture are rounded to minimize paste clogging. The solder paste coverage on the center paddle is 20% (this reduces the floating effects of the perimeter leads). The following illustration shows the stencil design.

Note: Lead-free solder paste (Sn/Ag/Cu—"no-clean", type 3 or type 4) is recommended. Careful process development is recommended because surface mount processes vary across companies.

Figure 4 • Stencil Design



The stencil should be laser-cut and electro-polished to facilitate paste release. The stencil aperture tolerance should be tightly controlled due to the small pitch. There should be a positive taper with a bottom stencil opening that is larger than the top. The recommended stencil thickness is 100 um (4 mils).

4.2 Package Placement

The package pick-and-place accuracy depends on the pick-and-place equipment. A machine with fine pitch placement accuracy is preferred. The following popular methods for package alignment using machine vision can be used:

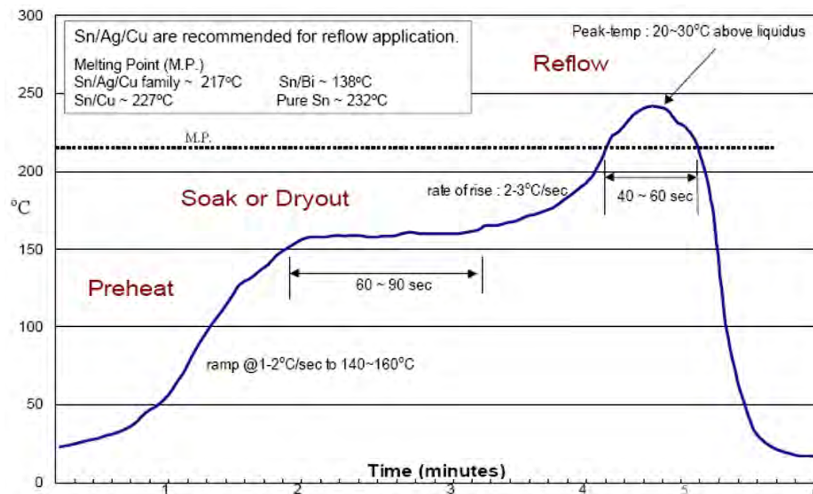
- Package silhouette (the vision system locates the package outline)
- Terminal recognition (the vision system locates the package lands)

The terminal recognition method is more accurate but slower.

4.3 Reflow Profile

Reflow profile and peak temperatures have a strong influence on the void formation after SMT. The solder paste supplier's recommended reflow profile should be followed because its specific to the flux formulation contained within the solder paste. A forced convection reflow oven with temperature uniformity of less than ±5 °C is recommended. The following illustration shows a typical reflow profile using Sn/Ag/Cu solder paste.

Figure 5 • Typical Reflow Profile Using Sn/Ag/Cu Solder Paste



4.4 Post Reflow Inspection

Post reflow inspection consists of X-ray sampling. The transmission X-ray will show the voids under the exposed paddle and any evidence of lead shorts.

5 Rework Procedure

For defects underneath the package, the whole package has to be removed and replaced. Rework of aQFN packages can be a challenge due to their small size. The reflow of adjacent parts is not desirable during rework, so the proximity of other components may further complicate this process. The following guidelines provide a starting point for the development of a successful rework process for these packages.

The rework process involves the following steps:

- Package removal
- Site redress
- Solder paste application
- Component placement
- Component attachment

Note: Prior to any rework, it is strongly recommended that the PCB assembly be baked for at least 4 hours at 125 °C to remove any residual moisture from the assembly.

5.1 Package Removal

The first step in component removal is the reflow of solder joints attaching component to the board. Ideally, the reflow profile for part removal should be the same as the one used for part attachment. However, the time above liquid can be reduced as long as the reflow is complete.

In the removal process, it is recommended to use a rework machine for better quality. The board should be heated from the bottom side using convective heaters, and hot gas or air should be used on the top side of the component. Special nozzles should be used to direct the heating in the component area, and heating of adjacent components should be minimized. Excessive airflow should also be avoided because this may cause the aQFN to skew.

5.2 Site Redress

After the component has been removed, the site needs to be cleaned properly. The residual solder must be removed by cleaning the lands with a solvent. The solvent is usually specific to the type of paste used in the original assembly and the paste manufacturer's recommendations should be followed.

5.3 Solder Paste Application

A miniature stencil specific to the package footprint is used for the solder paste printing. The stencil aperture should be aligned with the lands under 50x to 100x magnification. The stencil is lowered onto the PCB and the paste is deposited with a small squeegee blade. Alternatively, the mini stencil can also be used to print paste directly on the package lands.

5.4 Component Placement

Before placing the component, add some flux onto both the aQFN component and the PCB board. The aQFN packages are expected to have superior self-centering ability due to their small mass, and the placement of this package should be similar to that of QFNs. As the leads are on the underside of the package, split-beam optical system should be used to align the component on the motherboard. This will form an image of leads overlaid on the mating footprint and aid in proper alignment. The alignment should be done at 50x to 100x magnification. The placement machine should have the capability of allowing fine adjustments in the X, Y, and rotational axes.

5.5 Package Reflow

The original reflow profile used for the original attachment should be used for the reworked package.

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