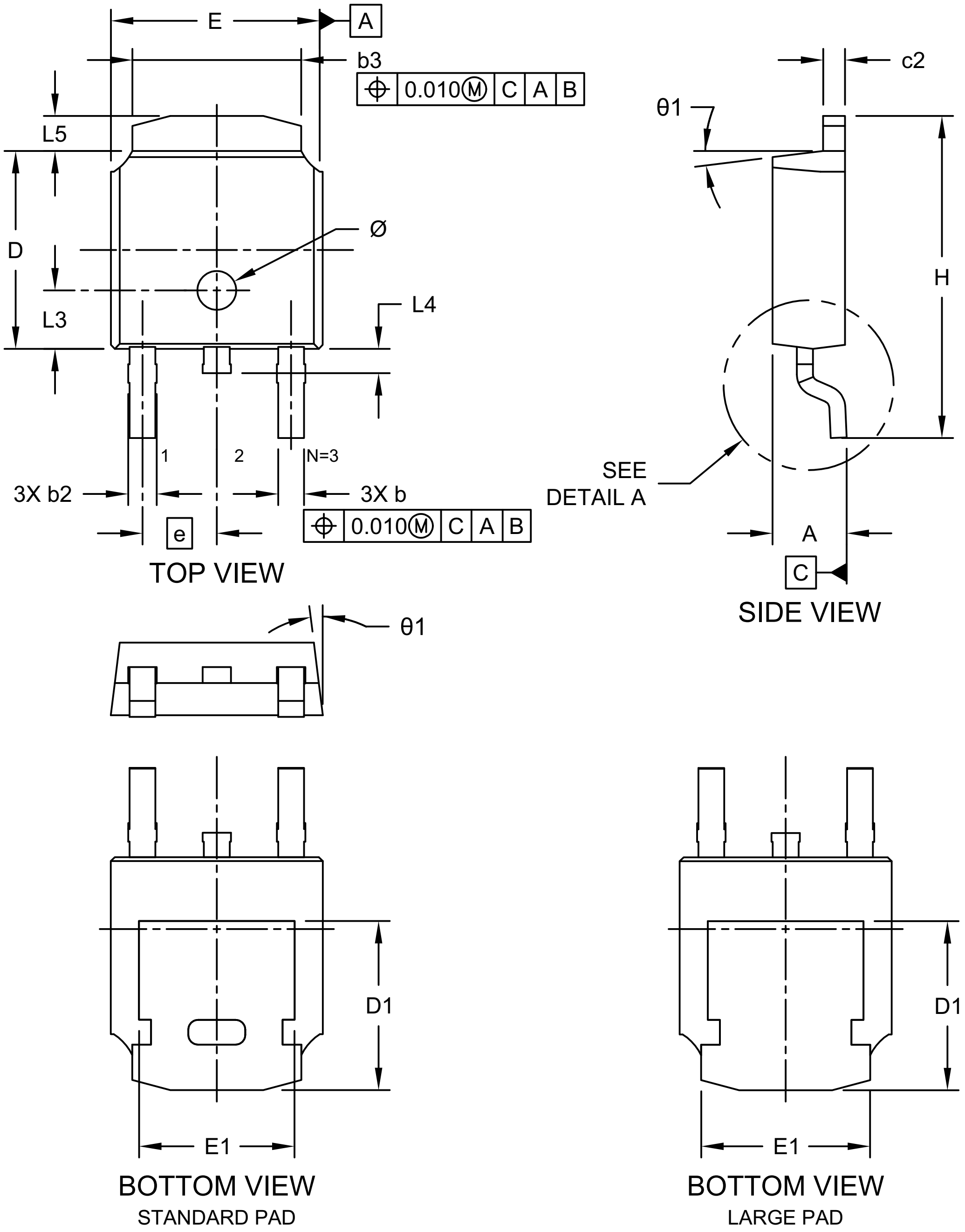
3-Lead Deca-Watt Package, TO-252 (EA) - [DPAK]; Supertex Legacy Package Code K4

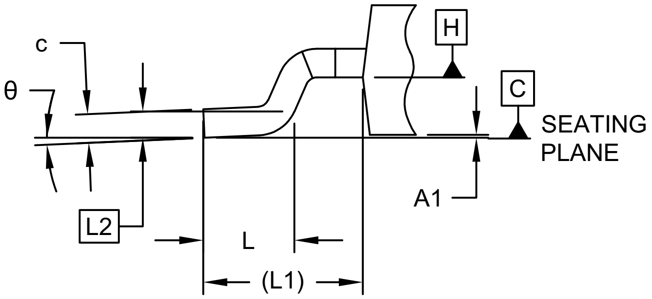
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



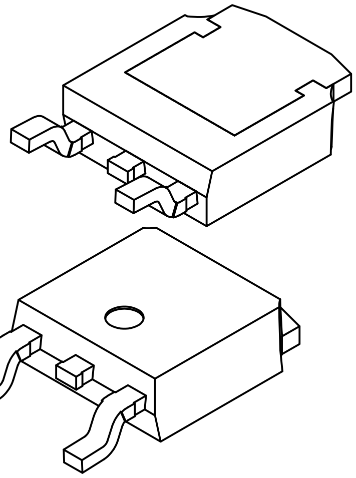
Microchip Technology Drawing C04-189 Rev C Sheet 1 of 2

3-Lead Deca-Watt Package, TO-252 (EA) - [DPAK]; Supertex Legacy Package Code K4

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL A
ROTATED 90°



Units	INCHES		
	MIN	NOM	MAX
N (Leads)	3		
e	.090 BSC		
A	.086	-	.094
A1	.000	-	.005
b	.028	-	.035
b2	.030	-	.045
c	.018	-	.024
c2	.018	-	.035
D	.235	.240	.245
D1	.205	-	-
E	.250	-	.265
E1	.170	-	-
H	.370	-	.410
L	.055	.060	.070
L1	.108 REF		
L2	.020 BSC		
L3	.065	-	.077
L4	.024	-	.035
L5	.035	-	.050
θ	1°	-	5°
θ1	7° REF		

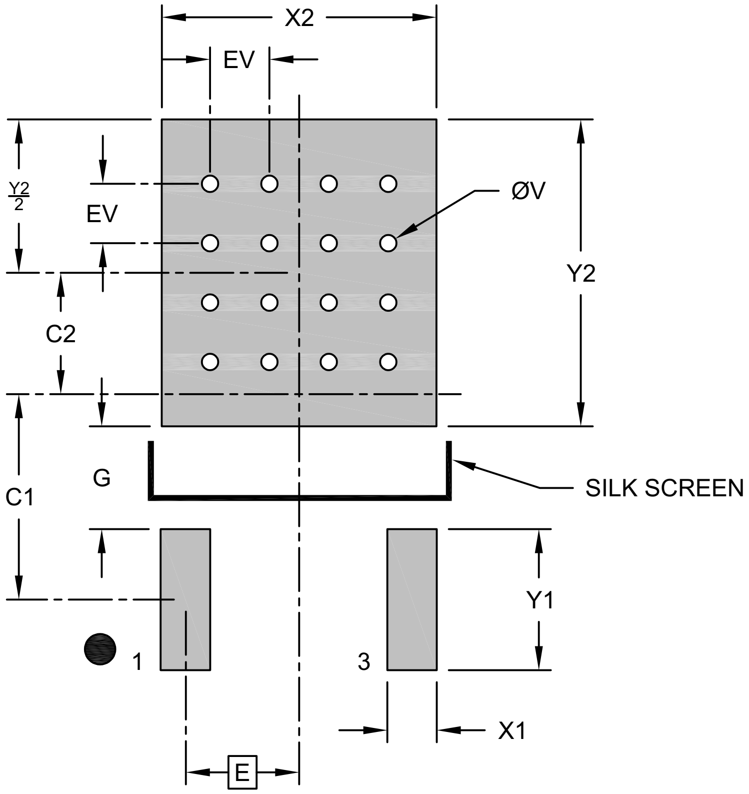
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-189 Rev C Sheet 1 of 2

3-Lead Deca-Watt Package, TO-252 (EA) - [DPAK]; Supertex Legacy Package Code K4

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		.090 BSC	
Center Pad Width	X2			.219
Center Pad Length	Y2			.244
Contact Pad Spacing	C1		.163	
Contact Pad Spacing	C2		.096	
Contact Pad Width (Xnn)	X1			.039
Contact Pad Length (Xnn)	Y1			.112
Contact Pad to Contact Pad (Xnn)	G	.412		
Thermal Via Diameter	V		.013	
Thermal Via Pitch	EV		.047	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2189 Rev C