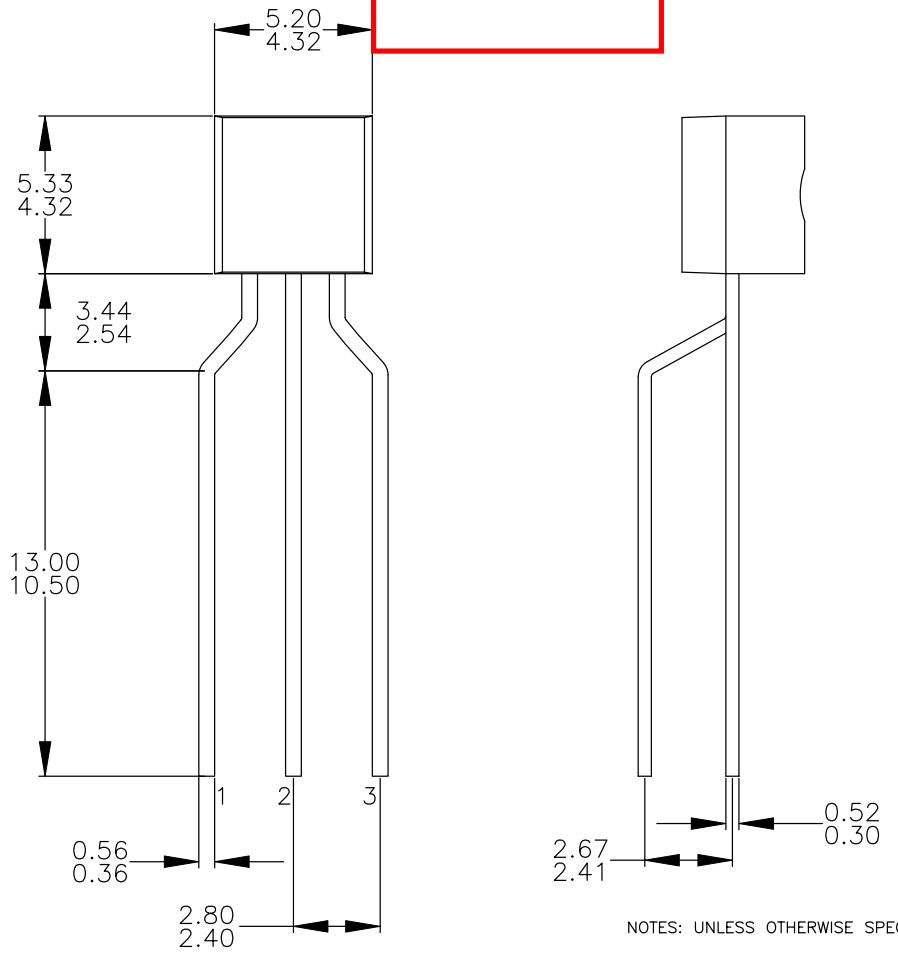
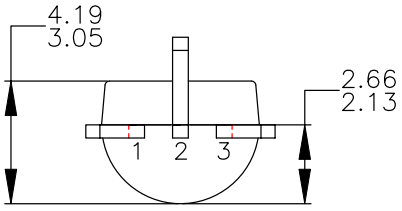
REVISIONS

NO.	DESCRIPTION	DATE	NAME/SITE
A	RELEASE TO DOCUMENT CONTROL	04MAR1995	JT/CB
2	RDRW FR NATIONAL TEMPLATE TO STD FSC MKT DWG TEMPLATE; CHG DIM REF FR DUAL DIM INCH[MM] TO SINGLE DIM MM; CHG MOLD BODY WIDTH FR 4.699 4.318 TO 5.33 4.32; CHG MOLD BODY HT FR 4.699 4.318 TO 5.33 4.32; REMOVE DAMBAR DIMS; ADD OVERALL BENDED LD LENGTH; CHG STRAIGHT LD DIM FR 13.00 12.00 TO 13.00 10.00; CHG LD PITCH FR 2.667 2.413 TO 2.80 2.40; CHG LD WIDTH FR 0.508 0.356 TO 0.56 0.36; REMOVE LD SURF TO MOLD SURF DIM; ADD MOLD BODY THICKNESS DIM; CHG PKG BOT TO LD SURF DIM FR 2.413 2.15 TO 2.66 2.13; REMOVE DRAFT ANGLE MOLD SURF DIMS; REMOVE EJECTOR PIN FEATURE & DIMS; CHG LD THICKNESS FR 0.483 0.304 TO 0.52 0.30; CHG LD BEND HT FR 2.667 2.413 TO 2.67 2.41; ADD NOTES SECTION.	26MAR2008	JC/FSCP

APPROVED
July-14-2008





NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M-1994.
D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	C	G	D	C	G	D
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:
P – BIPOLAR E – EMITTER D – DRAIN
F – JFET B – BASE S – SOURCE
M – DMOS C – COLLECTOR G – GATE

E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT-ZA03AREV2.

APPROVALS	DATE
DRAWN: J.U. COMPARATIVO JR.	03APR2008
CHECKED: L. GALERA	
APPROVED: M.R. GESTOLE	
G.S. BAJE	

PROJECTION INCH [MM]

FAIRCHILD SEMICONDUCTOR™

3LD,TO-92,MOLDED
TO-5 STD LD FORM
(J05Z OPTION)

SCALE	SIZE	DRAWING NUMBER	REV
1:1	N/A	MKT-ZA03A	2

FORMERLY: N/A SHEET : 1 OF 1